IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 3, 7, and 18 and ADD new claim 28 in accordance with the following:

1. (CURRENTLY AMENDED) A method of a digital frequency correction, comprising:

sampling a signal with a sampling cycle (k) and digitalized (x(k));

processing an N-step CORDIC algorithm so that a frequency of a signal (x(k)) is altered at a predetermined frequency;

representing the signal (x(k)) by a first vector comprising a first in-phase component (i_0) and a first quadrature component (q_0) in a complex I/Q plane;

imaging the first vector ~~by applying the CORDIC algorithm~~ onto a second vector with a second in-phase component (I_n) and a second quadrature component (Q_N) by applying a CORDIC algorithm to perform a vector rotation with a predetermined angle (z(k)), wherein the second vector represents a signal with an altered frequency and phase; and

composing ~~a~~ said predetermined angle (z(k)) of N different rotation angles (α_n), wherein each of the different rotation angles (α_n) are calculated according to $\arctan(2^{-n})$, n = 0, 1,..., N-1, and are respectively provided with a sign (σ_n) providing a direction of rotation.

2. (PREVIOUSLY PRESENTED) The method as recited in claim 1, wherein the predetermined angle (z(k)) is limited to a range of 0 to 2π, and where the predetermined angle (z(k)) is represented by a register value (w(k)), a bit width N_w prescribing the range of 0 to 2π for the predetermined angle (z(k)), a register value (w(k)) being calculated in each cycle (k) of the sampling cycle by an addition of a value (f·T/m), allocated to the predetermined angle (z(k)), and a register value w(k-1)) of the preceding cycle (k-1) of the sampling cycle, where an overflow of the register value (w(k)) is neglected.

3. (CURRENTLY AMENDED) The method as recited in claim 2, wherein the predetermined angle (z(k)) is limited to a range of $-\pi/2$ to $+\pi/2$, where a quadrant correction is carried out before the CORDIC algorithm, and the first in-phase component (i_0) and the first

quadrature component (q_0) are respectively multiplied by $(-1)^{2S}$, s = 0, 1.

4. (PREVIOUSLY PRESENTED) The method as recited in claim 3, wherein the bit width N_w of the register value (w(k)) comprises:

$$N_w \geq \log2(m) - \log2(\Delta f \cdot T),$$

where m comprises an oversampling factor of the signal (x(k)) and T represents a duration of a digital value of the signal (x(k)).

5. (PREVIOUSLY PRESENTED) The method as recited in claim 4, wherein a number N of operations of the CORDIC algorithm for a predetermined signal to phase noise ratio SNR and the bit width N_w of the register value (w(k)) comprises a following condition:

$$(SNR + 3)/6 \leq N \leq N_w - 2.$$

6. (PREVIOUSLY PRESENTED) The method as recited in claim 5, wherein two guard bits are provided in each operation of the CORDIC algorithm, and an input and output bit width of the CORDIC algorithm is at least greater than N + 2.

7. (CURRENTLY AMENDED) An apparatus of a digital frequency correction of a signal, which is sampled with a sample cycle (k) and is digitized (x(k)), comprising:

N micro-rotation blocks receiving a signal (i_0, q_0);

a sign table providing to each micro-rotation block a sign (σ_n) from a sign table~~,~~;

a register driving the sign table and supplying a register value (w(k));

a delay element; and

an adder ~~adds~~ adding a predetermined frequency value (f•T/m) to an output value of the delay element, outputting a result indicative thereof, and storing the result in the register, wherein the register value of a preceding cycle (k-1) is supplied to the delay element.

8. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 7, further comprising:

a quadrant correction block preceding the micro-rotation blocks, to which an input signal (s) is supplied, rotating the signal into a first or fourth quadrant of the complex I/Q plane and providing a vector (i_0, q_0) representing the signal being rotated.

9. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 8, wherein each

micro-rotation block comprises:

two shift registers shifting components of an input vector (I_n, Q_n) of the micro-rotation block by n bits and providing output values, and

two accumulators adding the components of the input vector (I_n, Q_n) to the output values of the shift registers, the output values of the shift registers being provided with the sign (σ_n) allocated to the respective micro-rotation block.

10. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 9, wherein the sign table comprises a read-only memory comprising 2^N (N - 2) bits, an XOR gate, and an inverter to produce a sign (σ_0, σ_1) for the first and second micro-rotation blocks and the input signal (s) for the quadrant correction block.

11. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 10, wherein the input signal (s) for the quadrant correction block is formed by a logical XOR operation on two lowest-value bits (w_0, w_1) of the register value (w(k)).

12. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 11, wherein the sign (σ_0) for the first micro-rotation block corresponds to a second bit (w_1) of the register value (w(k)).

13. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 12, wherein the sign (σ_1) for the second micro-rotation block corresponds to an inverted third bit (w_2) of the register value (w(k)).

14. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 13, the apparatus further comprising:

a receiver of a mobile radio device, comprising:

a baseband filter with stages filtering and processing a received baseband signal (x(k)); and

a last stage of the baseband filter to correct the frequency of the baseband signal x(k)).

15. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 14, further comprising:

an offset compensation of the baseband signal (x(k)) to remove DC portions.

16. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 14, wherein a GSM or UMTS mobile radio device comprises the receiver.

17. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 15, wherein the apparatus provides a communication system for digital IF mixing and/or frequency correction.

18. (CURRENTLY AMENDED) The method as recited in claim 1, wherein the predetermined angle (z(k)) is limited to a range of $-\pi/2$ to $+\pi/2$, where a quadrant correction is carried out before the CORDIC algorithm, and the first in-phase component (i_0) and the first quadrature component (q_0) are respectively multiplied by $(-1)^{2s}$, s = 0, 1.

19. (PREVIOUSLY PRESENTED) The method as recited in claim 2, wherein the bit width N_w of the register value (w(k)) comprises:

$$N_w \geq \log_2(m) - \log_2(\Delta f \cdot T),$$

where m comprises an oversampling factor of the signal (x(k)) and T represents a duration of a digital value of the signal (x(k)).

20. (PREVIOUSLY PRESENTED) The method as recited in claim 18, wherein a number N of operations of the CORDIC algorithm for a predetermined signal to phase noise ratio SNR and the bit width N_w of the register value (w(k)) comprises a following condition:

$$(SNR + 3)/6 \leq N \leq N_w - 2.$$

21. (PREVIOUSLY PRESENTED) The method as recited in claim 2, wherein a number N of operations of the CORDIC algorithm for a predetermined signal to phase noise ratio SNR and the bit width N_w of the register value (w(k)) comprises a following condition:

$$(SNR + 3)/6 \leq N \leq N_w - 2.$$

22. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 7, wherein each micro-rotation block comprises:

two shift registers shifting components of an input vector (I_n, Q_n) of the micro-rotation block by n bits and providing output values, and

two accumulators adding the components of the input vector (I_n, Q_n) to the output values of the shift registers, the output values of the shift registers being provided with the sign (σ_n) allocated to the respective micro-rotation block.

23. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 8, wherein the sign table comprises a read-only memory comprising 2^N (N - 2) bits, an XOR gate, and an inverter to produce a sign (σ_0, σ_1) for the first and second micro-rotation blocks and the input signal (s) for the quadrant correction block.

24. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 10, wherein the sign (σ_0) for the first micro-rotation block corresponds to a second bit (w_1) of the register value (w(k)).

25. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 10, wherein the sign (σ_1) for the second micro-rotation block corresponds to an inverted third bit (w_2) of the register value (w(k)).

26. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 11, wherein the sign (σ_1) for the second micro-rotation block corresponds to an inverted third bit (w_2) of the register value (w(k)).

27. (PREVIOUSLY PRESENTED) The apparatus as recited in claim 15, wherein a GSM or UMTS mobile radio device comprises the receiver.

28. (NEW) A method of correcting frequency of a signal recorded as a plurality of digital samples x(k) corresponding to a sampling cycle (k), comprising:

representing each of the plurality of digital samples x(k) by a first vector comprising a first in-phase component (i_0) and a first quadrature component (q_0) in a complex I/Q plane;

determining a plurality of angles z(k) by adding N different rotation angles (α_n), wherein each of the different rotation angles (α_n) are calculated according to $\arctan(2^{-n})$, n = 0, 1,..., N-1, and are respectively provided with a sign (σ_n) corresponding to a direction of rotation; and

imaging the first vector onto a second vector with a second in-phase component (I_n) and a second quadrature component (Q_N) by applying an N-step CORDIC algorithm using the plurality of angles z(k) to perform rotation of the first vector representing one of the plurality of samples x(k), so that the second vector represents digital samples of a corrected signal having a predetermined frequency.